The sequential read-out circuit 20 also includes a plurality of column switches 28, where there is one switch for each column. Each column switch is controlled by a control signal (e.g., SAMPLE_1, SAMPLE_2, .., SAMPLE_N). The sequential read-out circuit 20 also includes a charge transfer circuit 30 (also referred to herein as a charge conversion circuit) that is shared by the columns. The charge conversion circuit 30 converts the charge of each sample circuit of the columns in a sequential fashion.

The switches 28 can be implemented as a transistor as shown. However, it is noted that the switches 28 may be implemented by any circuit that selectively makes an electrical connection between the sample circuit 24 and the charge conversion circuit 30. The switches can include, for example, but is not limited to full transfer gates, NMOS transistors, PMOS transistors, and charge compensated transistor switches.

The charge conversion circuit 30 can be implemented as an amplifier as described in greater detail hereinafter with reference to FIG. 2. However, it is noted that the charge conversion circuit 30 may be implemented by any circuit that converts charge provided by the sample circuit 24 to an output voltage. The charge conversion circuit 30 can be implemented by, for example, fully differential operational amplifiers, simple single stage single ended operational amplifiers, and transimpedance amplifiers.

Exemplary Implementation of a System with a Sequential Read-Out Circuit

FIG. 2 is a schematic diagram illustrating an exemplary implementation of the system 10 of FIG. 1. The sequential read-out circuit 100 is coupled to an array 110 of photocells that are arranged in rows and columns. For example, the array 110 may include R rows and C columns.

In this example, the sequential readout circuit 100 is selectively connected to photocells (e.g., a first photocell 114) in a first column 118 through pass transistor_1 and photocells (e.g., a second photocell 124) in a second column 128 through pass transistor_2. It is noted that the sequential read-out circuit 100 is selectively connected to every column in the array 110 through a respective column switch circuit.

The sequential read-out circuit 100 includes a single amplifier 130 that is coupled to the first photocell 114 and the second photocell 124. The amplifier 130 is also referred to herein as a transfer amplifier (TA) 130 that transfers charge between the input and the output of the amplifier. The amplifier 130 processes each photocell in the array in a time-sequential manner (i.e., one photocell at a time). For example, the photocells may be processed (e.g., read-out) row-by-row, where each photocell in a respective row is processed one photocell at a time. Specifically, the amplifier 130 performs a difference function for each photocell.

For example, the amplifier 130 determines the difference between a reset voltage (V_{reset}) and a light voltage (V_{light}) for the first photocell 114. Once the first photocell 114 has been processed, the amplifier 130 determines the difference between a reset voltage (V_{reset}) and a light voltage (V_{light}) for the second photocell 124. This processing proceeds until all the photocells of the current row have been processed.

The amplifier 130 includes a first input 132, an output 134, an integration capacitor 136. The integration capacitor 136 includes a first electrode 138 for coupling to the first input 132 and a second electrode 139 for coupling to the output 134 of the amplifier 130. The amplifier 130 includes a charge transfer mode and a unity gain mode, which are described in greater detail hereinafter.

The sequential read-out circuit 100 can also include a switch 160 (e.g., a transistor) that is responsive to a reset signal (e.g., a TARST signal) for resetting the amplifier 130. As described in greater detail hereinafter with reference to FIG. 7, a first mechanism may be coupled to the input 132 and the output 134 of the amplifier for performing a level shift of the output of the amplifier 130. A second mechanism may be coupled to the input 132 and the output 134 of the amplifier for performing gain manipulation of the amplifier 130.

The sequential read-out circuit 100 also includes a first sample and hold circuit 140 that is coupled to the first photocell 114 for sampling and holding the output voltage of the first photocell 114. The first sample and hold circuit 140 includes a first sampling capacitor 144 and a first switch (e.g., transistor 148) that is coupled to the first sampling capacitor 144. The first switch 148 selectively forms an electrical connection between the first column and the input 132 of the amplifier 130 in response to a first control signal (e.g., SAMPLE_1).

The sequential read-out circuit 100 also includes a second sample and hold circuit 150 that is coupled to the second photocell 124 for sampling and holding the output voltage of the second photocell 124. The second sample and hold circuit 150 includes a second sampling capacitor 154 and a second switch (e.g., transistor 158) that is coupled to the second sampling capacitor 154. The second switch 158 selectively forms an electrical connection between the second column and the input 132 of the amplifier 130 in response to a second control signal (e.g., SAMPLE_2).

Photo Cell 300

FIG. 3 illustrates in greater detail an exemplary photo cell architecture that can be utilized in FIG. 1 according to one embodiment of the present invention. The cell 300 includes a photodiode (D1) for detecting light and responsive thereto for generating a voltage representation thereof. The cell 300 includes an integration node (hereinafter referred to as a Vlight node). The cell 300 also includes a first switch (SW1) that is coupled to the photodiode for resetting the integration node in response to a reset signal (RESET). The cell 300 includes a first transistor (N1) that is coupled to the integration node for shifting the level of the voltage at the integration node to a level-shifted voltage (B_{out}). The cell 300 also includes a second transistor (N2) that is coupled to the first transistor (N1) for reading out the level-shifted voltage in response to a read signal (RD). The output of the cell 300 is then provided to the sample circuit 24.

The photo-diode is modeled for ease of understanding by a current source Ilight, which represents the photo current that is generated in the reversed bias diode in response to the generation of electro- hole pairs by photon absorption by the silicon. This current is the signal that is of importance in the photodetector. The capacitor Cd + Cp represents the capacitance on the node Vlight. This capacitance includes the photodiode reversed bias capacitance and the parasitic capacitance on the node that includes interconnect capacitance, the diffusions of the SW1, and the input gate capacitance of N1.

The array may be utilized in one of a variety of different applications. These applications include, for example, but are not limited to, an optical mouse, scanner